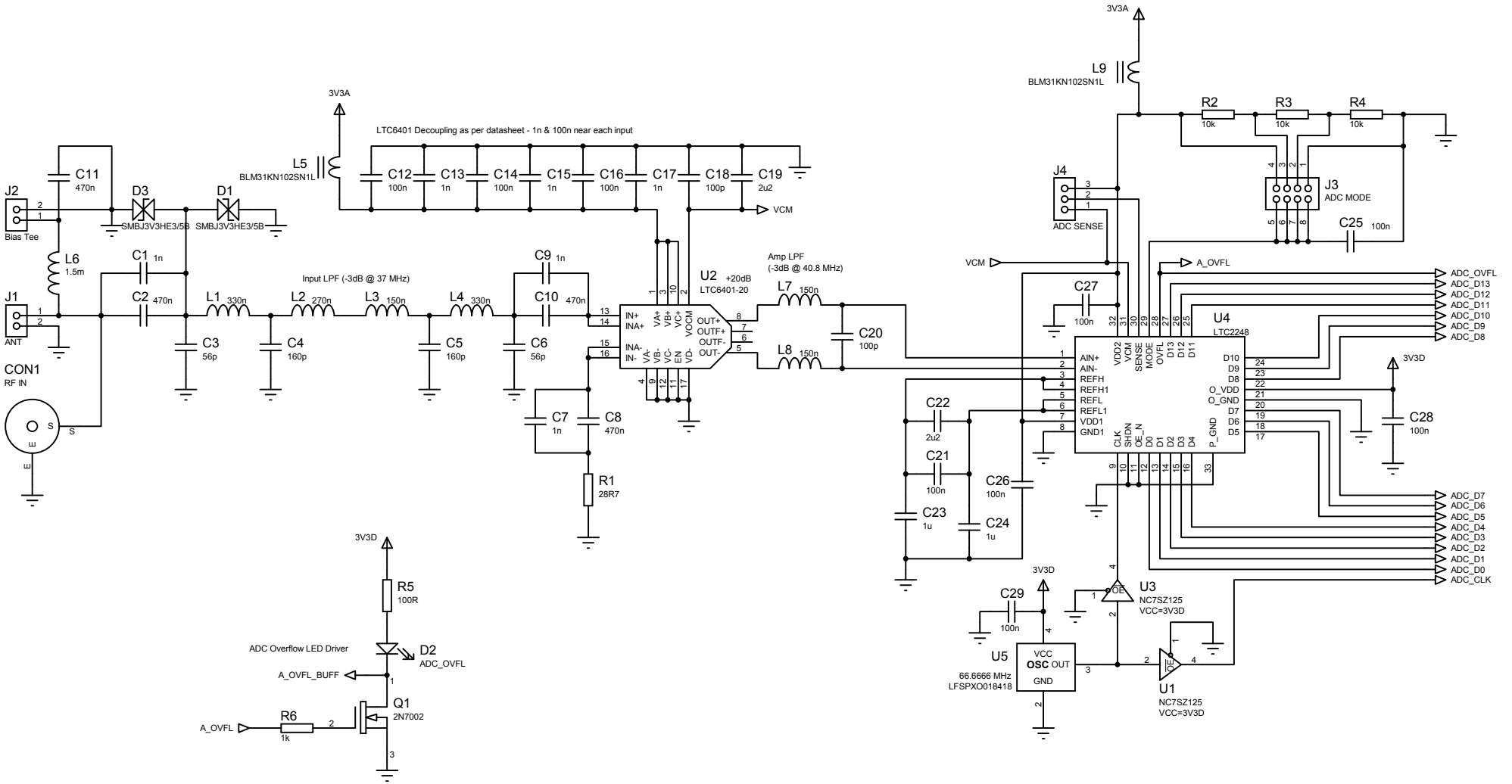


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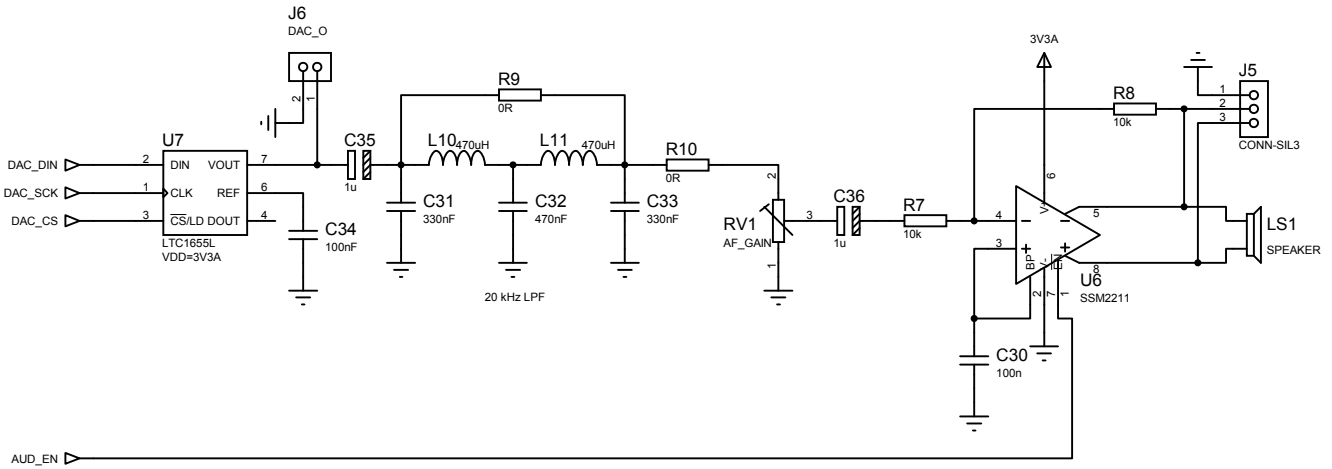
| FILE NAME: GS_FPGA_ADC 3.pdsprj | DATE: 9/16/2018 |
| DESIGN TITLE: ARTY FPGA SDR | PAGE: 1 of 4 |
| PATH: \\BOXSVR\george\Electronics\FPGA\Analog_Front_End\GS_FPGA_ADC 3\RF Input.SchDoc | |
| BY: George M1GEO REV: B | TIME: 1:35:54 AM |

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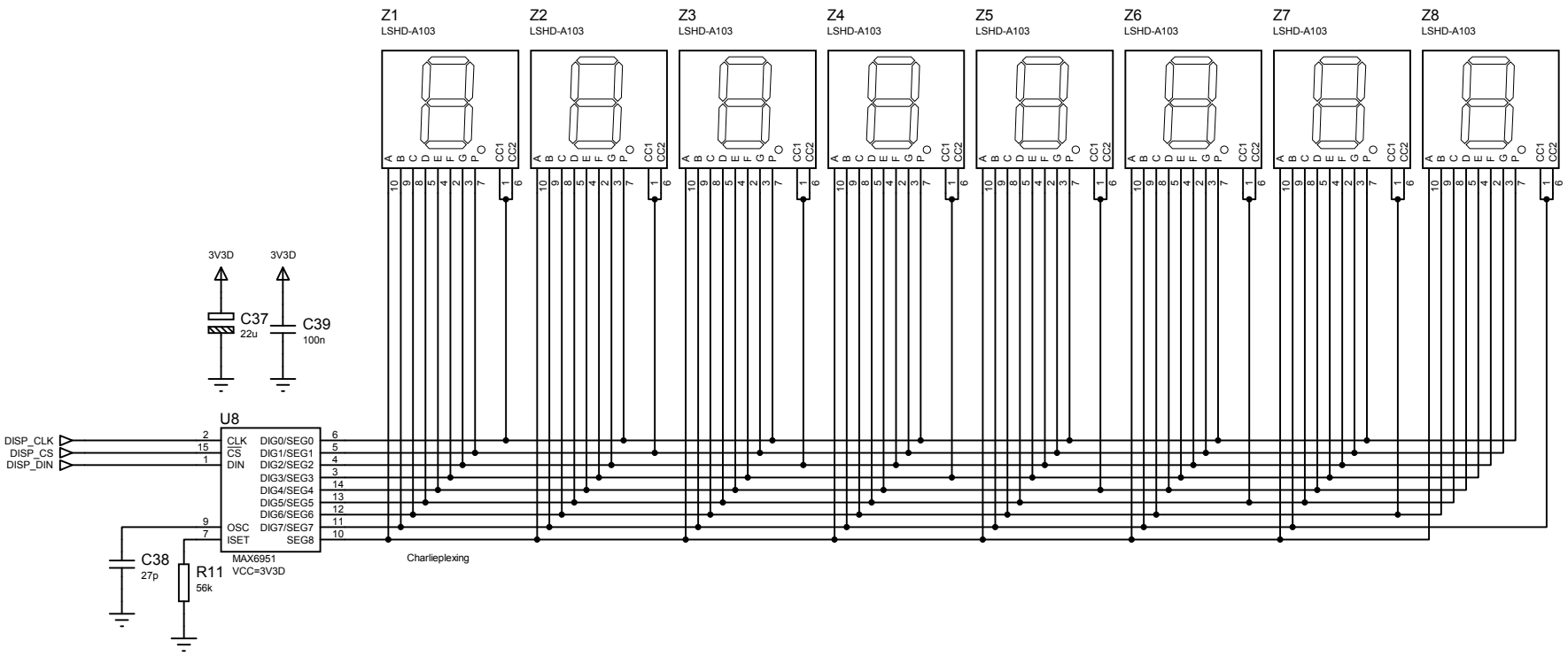
| DESIGN TITLE: ARTY FPGA SDR | PAGE: 2 of 4 |
| PATH: \\VBOXSVR\george\Electronics\FPGA\Analog_Front_End\GS_FPGA_Audio_Output_DAC | |
| BY: George M1GEO REV: B | TIME: 1:35:54 AM |

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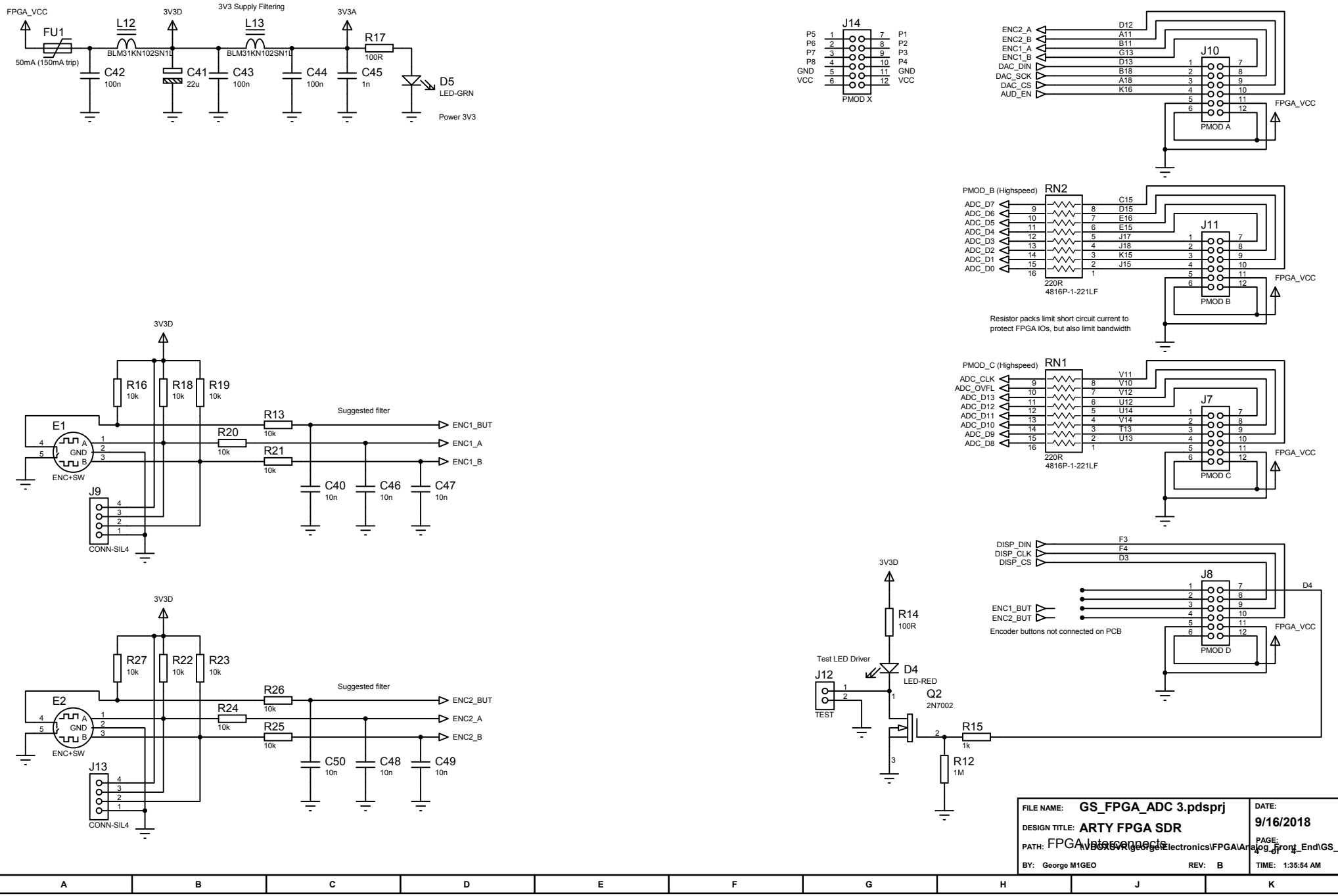
| FILE NAME: GS_FPGA_ADC 3.pdsprj | DATE: 9/16/2018 |
| DESIGN TITLE: ARTY FPGA SDR | PAGE: 3 of 4 |
| PATH: \\BDXSVR\george\Electronics\FPGA\Analog_Front_End\GS_FPGA_ADC 3\LED Display | |
| BY: George M1GEO REV: B | TIME: 1:35:54 AM |


3V3 Supply Filtering
FPGA_VCC
FU1
50mA (150mA trip)
L12
BLM31KN102SN1L
L13
BLM31KN102SN1L
3V3D
3V3A
R17
100R
C42 100n
C41 22u
C43 100n
C44 100n
C45 1n
D5
LED-GRN
Power 3V3
J14
PMOD X
P5 P6 P7 P8 GND VCC
P1 P2 P3 P4 GND VCC
J10
PMOD A
ENC2_A ENC2_B ENC1_A ENC1_B DAC_DIN DAC_SCK DAC_CS AUD_EN
D12 A11 B11 G13 D13 B18 A18 K16
FPGA_VCC
PMOD_B (Highspeed)
RN2
220R
4816P-1-221LF
ADC_D7 ADC_D6 ADC_D5 ADC_D4 ADC_D3 ADC_D2 ADC_D1 ADC_D0
C15 D15 E16 E15 J17 J18 K15 J15
J11
PMOD B
Resistor packs limit short circuit current to protect FPGA IOs, but also limit bandwidth
PMOD_C (Highspeed)
RN1
220R
4816P-1-221LF
ADC_CLK ADC_OVFL ADC_D13 ADC_D12 ADC_D11 ADC_D10 ADC_D9 ADC_D8
V11 V10 V12 U12 U14 V14 T13 U13
J7
PMOD C
3V3D
R16 10k
R18 10k
R19 10k
E1
ENC+SW
R13 10k
R20 10k
R21 10k
Suggested filter
ENC1_BUT
ENC1_A
ENC1_B
C40 10n
C46 10n
C47 10n
J9
CONN-SIL4
R27 10k
R22 10k
R23 10k
E2
ENC+SW
R26 10k
R24 10k
R25 10k
Suggested filter
ENC2_BUT
ENC2_A
ENC2_B
C50 10n
C48 10n
C49 10n
J13
CONN-SIL4
DISP_DIN DISP_CLK DISP_CS
F3 F4 D3
J8
PMOD D
ENC1_BUT ENC2_BUT
Encoder buttons not connected on PCB
D4
Test LED Driver
J12
TEST
R14 100R
D4 LED-RED
Q2 2N7002
R15 1k
R12 1M
FILE NAME: GS_FPGA_ADC 3.pdsprj
DESIGN TITLE: ARTY FPGA SDR
PATH: \\VBOXSVR\george\Electronics\FPGA\Analog_Front_End\GS_FPGA_Interconnects
BY: George M1GEO
REV: B
DATE: 9/16/2018
PAGE: 4 of 4
TIME: 1:35:54 AM