A 0.6V All-Digital Body-Coupled Wakeup Transceiver for IoT Applications

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Abstract

A body-coupled symmetric wakeup transceiver is proposed for always-on device discovery in IoT applications requiring security and low-power consumption. The wakeup transceiver (WTRx) is implemented in 65nm CMOS, using digital logic cells and operates at 0.6V. A directly-modulated open-loop DCO generates an OOK-modulated 10MHz carrier, with a frequency-locked loop for intermittent calibration. A passive receiver incorporates a digital IO cell as hysteretic comparator, with a two-phase correlator bank. A novel MAC scheme allows for duty-cycling in both transmitter and receiver. Measured power consumption is 3.54μW, with sensitivity of 88mV and maximum wakeup latency of 150ms.

Keywords: BCC, wakeup, BCC, OOK, WTRx, FLL, DCO

Introduction

Emerging Internet of Things (IoT) applications demand extremely energy-efficient wireless communications. State of the art RF personal area radios achieve high energy-efficiency for wireless data transfer. However, before exchanging data, two IoT devices must first be able to discover each other. The key requirements for device discovery are low "always-on" power consumption (c.f. energy/bit), detection latency below the human perception limit (~150ms), and a means to select the intended device to interact with from all within range. Since the RF channel is not well localized, a selection step is required by the user to choose a device from a list of those within range.

In this work, we propose a Body-Coupled Communication (BCC) wakeup transceiver (WTRx) as an improved method to perform device discovery. BCC uses the human body to couple a very localized electric field between nodes in close proximity to the skin [1-4]. The BCC channel exhibits low loss and high SNR in low-frequency bands (1-40 MHz) [1]. Using BCC instead of RF for discovery/wakeup offers four key benefits: 1) channel localization for improved security, as the electric field is confined to the body and does not radiate, 2) intuitive user experience, as the act of touching another device or person can initiate the pairing operation in a seamless manner, 3) avoidance of transmitter power amplifier as there is no need to drive a 50Ω antenna, and 4) low-power consumption, due to low $Fc \bullet Ceff \bullet Vdd^2$ switching power and very modest selectivity and sensitivity requirements.

Symmetric Wakeup System

Wakeup radios are conventionally simplex receivers only, without stringent constraints on the transmitter. In contrast, the WTRx is a symmetric half-duplex transceiver, which alternates between transmitting and receiving across the BCC channel, such that two un-synchronized nodes can detect each other. To reduce system power consumption without exceeding the target wakeup detection latency of 150ms, we use a medium access control (MAC) layer derived from preamble sampling [5] to enable duty cycling in the transceiver. Fig. 1 outlines the scheme. Each node repeats a sequence of four phases: three receive (T_{RX}=20ms), followed by one transmit (T_{TX}=40ms). Each phase starts with a channel check assessment (CCA), which looks for the "on" modulated carrier in an 8 symbol (2ms) time period. During T_{RX}, if no carrier is found (CCA==0), the transceiver can sleep for the remainder of the phase. If CCA==1, then the correlator is started and runs until wakeup detection, or the end of T_{RX}. During transmit, the node must still first perform the CCA to ensure that the channel is not in use. If CCA==1, then the correlator will run for the period, as above. Otherwise, the transmitter sends a 31b correlation sequence repeatedly for a 20ms burst. The proposed approach allows the WTRx to be idle 54% of the time, drastically reducing always-on power.

Circuit Design

The WTRx is implemented as an AHB peripheral on a 65nm SoC (Fig. 2). The whole peripheral runs from a single 0.6V supply, is implemented in standard digital library cells using an automated place and route tool flow. The whole design is described in Verilog, mostly synthesizable with some cell netlists. A single insulated electrode is used for transmission and reception at a carrier frequency of 10MHz. On-Off Keying (OOK) is used to allow for simple non-coherent demodulation. The 4kHz symbol clock is derived from a 32kHz SoC crystal oscillator (XO) clock (external to the WTRx).

Fig. 3 shows the transmit path, which is based around a frequency-locked loop (FLL). The single-ended CMOS digitally-controlled oscillator (DCO) consists of 8 stages, each consisting of 8 parallel unit-coded tri-state buffers. The FLL is activated after reset (using a fast SAR controller) and before each transmission (using an accurate bang-bang (BB) loop) to lock the DCO to the 10MHz carrier frequency, as measured against the XO reference. Once the loop is locked, it becomes idle, and the DCO is used open-loop during the burst, as the receiver has modest selectivity and is relatively insensitive to frequency error. To reduce DCO power, OOK signaling is achieved using direct modulation of the DCO, which incorporates a latch-based glitchless enable and offers relatively negligible startup delay. A standard digital IO cell drives the DCO output into an off-chip single-ended LC tank circuit with passive voltage gain of 6dB when loaded.

The resonant circuit in the transmitter achieves sufficient signal swing at the receiver for a passive envelope detector, without front-end gain. Hence, the receiver consists of discrete diodes and a standard digital IO cell acting as a comparator. The rail-to-rail output of the IO cell is sampled using two phases (rising and falling edges) of the 4kHz symbol clock, to avoid explicit symbol alignment. Each phase drives a separate 31-stage correlator bank, with programmable code. A pair of threshold detectors are then used to detect wakeup from either of the correlators, and an interrupt is generated to the on-chip Cortex-M0 microcontroller (MCU). A simple timer-driven state-machine and small register file are included for MAC sequencing without waking the MCU.

Measurement Results

Fig. 4 shows transmitter baseband data and OOK carrier. At

0.6V the DCO fractional BW is 25% and average gain is 39kHz/bit, allowing frequency accuracy <<1% in lock condition. Receiver sensitivity was measured to be 88mVpp and is set by the hysteresis of the digital IO cell circuit. The receiver input signal swing was measured when transmitting across the body from one hand to the other, with an additional material between one hand and the insulated electrode (Fig. 4). The sensitivity was sufficient with margin as long as the hand was touching the electrode. Measured receiver jitter is negligible at 4kHz symbol rate (Fig. 5).

The WTRx peripheral is "always-on" in the SoC, so power is critical (rather than energy/bit). As the design is digital, power consumption scales quadratically with supply voltage (Fig. 6). At the 0.6V design point (DCO center frequency of 10MHz), power dissipation is 5µW (Rx) and 6.5µW (Tx), with 0.5µW leakage power in the idle state. With the duty-cycling provided by the scheme of Fig. 1, power consumption reduces to 3.54µW.

Previously published BCC transceivers [2-4] are focused on data transfer and achieve high data rates and sensitivities at relatively high power (Fig. 7). In contrast, WTRx demonstrates symmetric wakeup BCC with very low area and power for secure device discovery in IoT applications.

References

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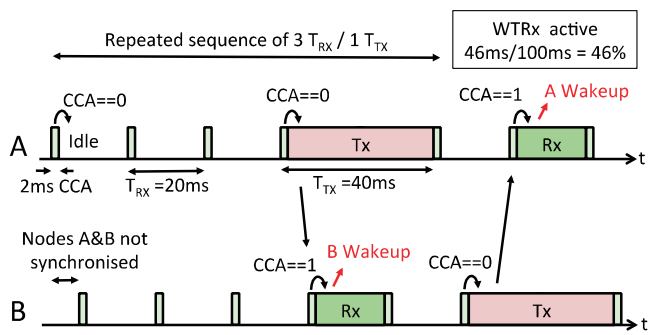

Fig. 1: Symmetric wakeup MAC scheme, (simplified timing does not include FLL lock time).

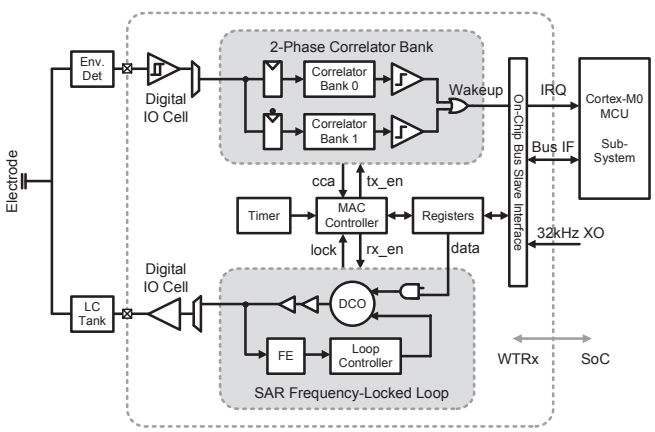

Fig. 2: Transceiver block diagram. The MAC controller sequences FLL locking as well as Tx and Rx signal paths.

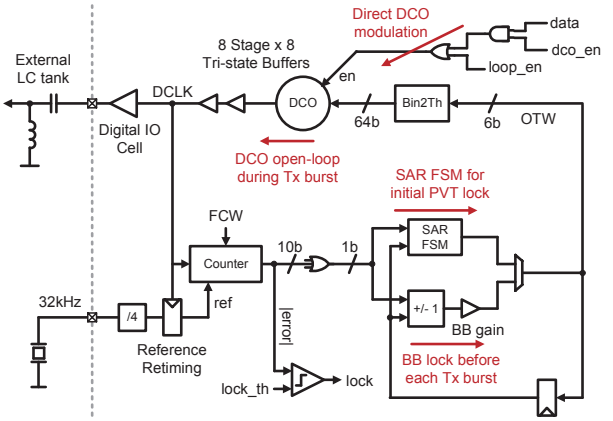

Fig. 3: All-digital FLL with SAR and BB loop controllers and OOK modulation.

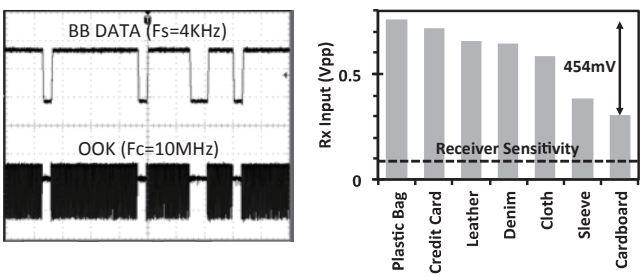

Fig. 4: Measured Tx waveforms (left), and Rx swing (right) from one hand to the other, with margin to min. sensitivity.

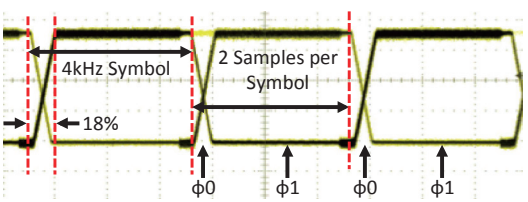

Fig. 5: Wide eye-opening at 4kHz allows for robust 2-phase correlator without clock-data recovery or Manchester coding.

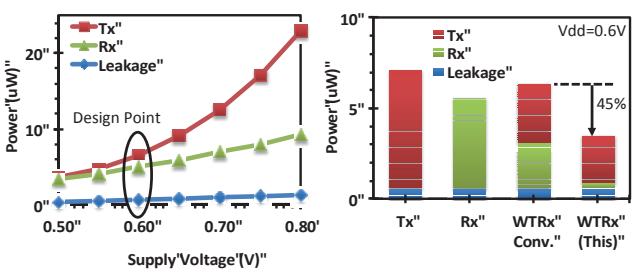

Fig. 6: Power breakdown over voltage (left); and function (right).

	[2] ISSCC'06	[3] ISSCC'09	[4] ISSCC'13	WTRx
Usage	Data	Data	Data	Wakeup
Carrier Freq. [MHz]	0.1–100	30–70	21	8.5–11
Symbol Rate [MHz]	2	8.5	1.3	0.004
Modulation	NRZ	NRZ	FSDT	OOK
Power [µW]	200	2300	5500	3.54 *
Sensitivity [mV]	10	0.35	-	88
Supply Voltage [V]	1	1.2	-	0.6
Process [nm]	250	180	130	65
Area [mm²]	0.85	0.19	12.5	0.01 *

* Not including SoC Crystal Oscillator

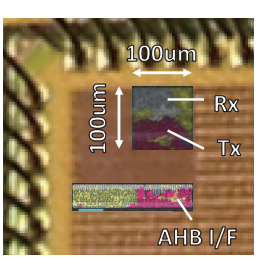

Fig. 7: Comparing with published BCC silicon shows WTRx is the first BCC symmetric wakeup transceiver, offering a much lower performance/power consumption trade-off for device discovery.